

Circuit / IO Architect

- ▶ Experience with high speed DDR / GDDR IO design
- ▶ Familiarity with Analog Components on Silicon, concerns / problems associated with high speed I/O buffers, DLLs / PLLs, etc.
- ▶ Experience in using CAD tools such as Cadence Virtuoso, HSpice, Magma Blast tools for logic / physical synthesis
- ▶ Deep knowledge of high speed IO and clocking, power delivery, chip construction and physical verification
- ▶ Will work closely with RTL design team, in house designers, IP suppliers and design service providers to deliver multiple chips with high speed IO into high volume production
- ▶ MSEE desired
- ▶ 7+ years related experience